PATENT
Attorney Docket No. 401557/FUKAMI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

OHNAKADO et al.

Application No. Unassigned

Art Unit: Unassigned

Examiner: Unassigned

Filed: February 6, 2002

For: PROTECTION CIRCUIT AGAINST ELECTROSTATIC DISCHARGE

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE TITLE:

Replace the title with:

CIRCUIT PROTECTING AGAINST ELECTROSTATIC DISCHARGE

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 11 with:

A discharge phenomenon that occurs between an electrostatically charged object and another object when they contact each other is called ESD (electrostatic discharge). An ESD to a semiconductor device may destroy the semiconductor device. The ESD can be typically modeled into three types: (a) HBM (Human Body Model) modeling discharge from a charged human body to a semiconductor device; (b) MM (Machine Model) modeling discharge from a charged apparatus to a semiconductor device; and (c) CDM (Charge Device Model) modeling discharge of electric charges on a semiconductor device to a grounded object.

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Replace the paragraph beginning at page 1, line 30 with:

As shown in Fig. 12, when the ESD occurs, a high current is applied to the semiconductor device in a short time. This may possibly cause "thermal breakdown", blowing of an interconnection line or the like by Joule heating. Particularly, when an MIS (Metal Insulator Semiconductor) transistor structure, the mainstream of the recent LSI (Large Scale Integration) silicon (Si) devices, is used, the gate insulation film of the MIS transistor is likely to be dielectrically broken down when a high electric field is applied thereto due to the ESD. The destruction or breakdown of an element due to the ESD is a significant problem.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A semiconductor device comprising:
an internal circuit;
a pad;
a signal transmission line coupled between said internal circuit and said pad, for transmitting a high frequency signal between said pad and said internal circuit;
a bypass transmission line connected between a first node of said signal transmission line and a first power supply node, for transmitting at least a signal component higher in frequency than the high frequency signal; and
a first surge conducting element connected between a second node of said signal transmission line and the first power supply node, for causing a current to flow between the second node and the first power supply node when a voltage at the first node exceeds a prescribed voltage level, the second node being located between the first node and the internal circuit.

2. (Amended) The semiconductor device according to claim 1, wherein said first surge conducting element includes a PN junction coupled in a reverse direction, viewed from the second node toward the first power supply node.

3. (Amended) The semiconductor device according to claim 1, wherein said first surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to the first power supply node, and a second conduction node connected to the second node.

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4. (Amended) The semiconductor device according to claim 1, wherein said first surge conducting element includes a diode element connected in a reverse direction viewed from the second node.

5. (Amended) The semiconductor device according to claim 1, further comprising a second surge conducting element connected between a third node of said signal transmission line and a second power supply node, and rendered conductive when a voltage at the third node exceeds a voltage level applied in a normal operation, the third node being located on said signal transmission line between the first node and said internal circuit.

6. (Amended) The semiconductor device according to claim 5, wherein said second surge conducting element includes a PN junction coupled in a reverse direction viewed from the third node toward the second power supply node.

7. (Amended) The semiconductor device according to claim 5, wherein said second surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to the second power supply node, and a second conduction node connected to the third node.

8. (Amended) The semiconductor device according to claim 5, wherein said second surge conducting element includes a diode element connected to the third node in a reverse direction viewed from the third node.

9. (Amended) The semiconductor device according to claim 1, further comprising a capacitor connected between the second node and said internal circuit.

10. (Amended) The semiconductor device according to claim 1, further comprising a clamp circuit connected between the first power supply node and a second power supply node, for holding a voltage difference between the first and second power supply nodes so as not to exceed a prescribed voltage level.

11. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit clamps the voltage difference between the first and second power supply nodes to a voltage level lower than a breakdown voltage of a diffusion layer of a second conductivity type located on a surface of a substrate region of a first conductivity type.

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12. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to the first power supply node, and a second conduction node connected to the second power supply node.

13. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a back gate and a first conduction node connected together to the second power supply node, and a second conduction node connected to the first power supply node.

14. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit includes at least one first diode element connected between the first power supply node and the second power supply node in a forward direction viewed from the first power supply node, and at least one second diode element connected between the second power supply node and the first power supply node in a forward direction viewed from the second power supply node.

15. (Amended) The semiconductor device according to claim 1, wherein the first power supply node is a ground node.

16. (Amended) The semiconductor device according to claim 1, wherein said bypass transmission line is a quarter wavelength transmission line having a length substantially equal to one quarter of a wavelength at an operation frequency of said internal circuit.

IN THE ABSTRACT:

Replace the Abstract with:

ABSTRACT OF THE DISCLOSURE

A quarter wavelength transmission line is provided between a signal transmission line for transmitting a high frequency signal and a ground node. The quarter wavelength transmission line has a length equal to a quarter of an effective wavelength of an operation frequency of a semiconductor device. A surge absorbing element is connected between the quarter wavelength transmission line and an internal circuit. The signal transmission line is coupled to the internal circuit through a capacitor. A clamp circuit is provided between a power supply line and a ground line. The clamp circuit clamps the voltage difference between the power supply line and the ground line to a prescribed voltage level or less. A

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high frequency semiconductor device is produced, preventing breakdown of an internal circuit element due to an electrostatic discharge phenomenon (ESD) without degrading high frequency characteristics.

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REMARKS

The foregoing Amendment corrects translational errors and conforms the claims to United States practice. No new matter is added.

Respectfully submitted,

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AMENDMENTS TO SPECIFICATION, CLAIMS AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 1, line 11:

A discharge phenomenon that occurs between an electrostatically charged object and another object when they contact each other is called ESD (electrostatic discharge). ~~The~~ An ESD to a semiconductor device may ~~destruct~~ destroy the semiconductor device. The ESD can be typically modeled into three types: (a) HBM (Human Body Model) modeling discharge from a charged human body to a semiconductor device; (b) MM (Machine Model) modeling discharge from a charged apparatus to a semiconductor device; and (c) CDM (Charge Device Model) modeling discharge of electric charges ~~charged itself in a semiconductor~~ device to a grounded object.

Amendments to the paragraph beginning at page 1, line 30:

As shown in Fig. 12, when the ESD occurs, a high current is applied to the semiconductor device in a short time. This may possibly cause "thermal breakdown", blowing of an interconnection line or the like by Joule ~~heat~~ heating. Particularly, when an MIS (Metal Insulator Semiconductor) transistor structure, the mainstream of the recent LSI (Large Scale Integration) silicon (Si) devices, is used, the gate insulation film of the MIS transistor is likely to be dielectrically broken down when a high electric field is applied thereto due to the ESD. The destruction or breakdown of an element due to the ESD is ~~significantly great~~ a significant problem.

Amendments to existing claims:

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1. (Amended) A semiconductor device~~,~~ comprising:

an internal circuit;

a pad;

a signal transmission line coupled between said internal circuit and ~~a~~ said pad, for transmitting a high frequency signal between said pad and said internal circuit;

a bypass transmission line connected between a first node of said signal transmission line and a first power supply node, for transmitting at least a signal component ~~that is~~ higher in frequency than ~~said~~ the high frequency signal; and

a first surge conducting element connected between a second node of said signal transmission line and ~~said~~ the first power supply node, for causing a current to flow between ~~said~~ the second node and ~~said~~ the first power supply node when a voltage at ~~said~~ the first node exceeds a prescribed voltage level, ~~said~~ the second node being ~~provided~~ located between ~~said~~ the first node and ~~said~~ the internal circuit.

2. (Amended) The semiconductor device according to claim 1, wherein said first surge conducting element includes a PN junction coupled in a reverse direction, viewed from ~~said~~ the second node toward ~~said~~ the first power supply node.

3. (Amended) The semiconductor device according to claim 1, wherein said first surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to ~~said~~ the first power supply node, and a second conduction node connected to ~~said~~ the second node.

4. (Amended) The semiconductor device according to claim 1, wherein said first surge conducting element includes a diode element connected in a reverse direction viewed from ~~said~~ the second node.

5. (Amended) The semiconductor device according to claim 1, further comprising a second surge conducting element connected between a third node of said signal transmission line and a second power supply node, and rendered conductive when a voltage at ~~said~~ the third node exceeds a voltage level applied in a normal operation, ~~said~~ the third node being ~~provided~~ located on said signal transmission line between ~~said~~ the first node and said internal circuit.

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6. (Amended) The semiconductor device according to claim 5, wherein said second surge conducting element includes a PN junction coupled in a reverse direction viewed from ~~said~~ the third node toward ~~said~~ the second power supply node.

7. (Amended) The semiconductor device according to claim 5, wherein said second surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to ~~said~~ the second power supply node, and a second conduction node connected to ~~said~~ the third node.

8. (Amended) The semiconductor device according to claim 5, wherein said second surge conducting element includes a diode element connected to ~~said~~ the third node in a reverse direction viewed from ~~said~~ the third node.

9. (Amended) The semiconductor device according to claim 1, further comprising a capacitor connected between ~~said~~ the second node and said internal circuit.

10. (Amended) The semiconductor device according to claim 1, further comprising a clamp circuit connected between ~~said~~ the first power supply node and a second power supply node, for holding a voltage difference between the first and second power supply nodes so as not to exceed a prescribed voltage level.

11. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit clamps ~~said~~ the voltage difference between ~~said~~ the first and second power supply nodes to a voltage level lower than a breakdown voltage of a diffusion layer of a second conductivity type ~~formed~~ located on a surface of a substrate region of a first conductivity type.

12. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to ~~said~~ the first power supply node, and a second conduction node connected to ~~said~~ the second power supply node.

13. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a back gate and a first conduction node connected together to ~~said~~ the second power supply node, and a second conduction node connected to ~~said~~ the first power supply node.

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14. (Amended) The semiconductor device according to claim 10, wherein said clamp circuit includes at least one first diode element connected between ~~said~~ the first power supply node and ~~said~~ the second power supply node in a forward direction viewed from ~~said~~ the first power supply node, and at least one second diode element connected between ~~said~~ the second power supply node and ~~said~~ the first power supply node in a forward direction viewed from ~~said~~ the second power supply node.

15. (Amended) The semiconductor device according to claim 1, wherein ~~said~~ the first power supply node is a ground node.

16. (Amended) The semiconductor device according to claim 1, wherein said bypass transmission line is a quarter wavelength transmission line having a length substantially equal to ~~a~~ one quarter of ~~an effective~~ a wavelength ~~of~~ at an operation frequency of said internal circuit.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

A quarter wavelength transmission line is provided between a signal transmission line for transmitting a high frequency signal and a ground node. The quarter wavelength transmission line has a length equal to a quarter of an effective wavelength of an operation frequency of a semiconductor device. A surge absorbing element is connected between the quarter wavelength transmission line and an internal circuit. The signal transmission line is coupled to the internal circuit through a capacitor. A clamp circuit is provided between a power supply line and a ground line. The clamp circuit clamps the voltage difference between the power supply line and the ground line to a prescribed voltage level or less. A high frequency semiconductor device is ~~thus implemented which is capable of~~ produced, preventing breakdown of an internal circuit element due to an electrostatic discharge phenomenon (ESD) without degrading high frequency characteristics.

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PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A semiconductor device comprising:

an internal circuit;

a pad;

a signal transmission line coupled between said internal circuit and said pad, for transmitting a high frequency signal between said pad and said internal circuit;

a bypass transmission line connected between a first node of said signal transmission line and a first power supply node, for transmitting at least a signal component higher in frequency than the high frequency signal; and

a first surge conducting element connected between a second node of said signal transmission line and the first power supply node, for causing a current to flow between the second node and the first power supply node when a voltage at the first node exceeds a prescribed voltage level, the second node being located between the first node and the internal circuit.

2. The semiconductor device according to claim 1, wherein said first surge conducting element includes a PN junction coupled in a reverse direction, viewed from the second node toward the first power supply node.

3. The semiconductor device according to claim 1, wherein said first surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to the first power supply node, and a second conduction node connected to the second node.

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4. The semiconductor device according to claim 1, wherein said first surge conducting element includes a diode element connected in a reverse direction viewed from the second node.

5. The semiconductor device according to claim 1, further comprising a second surge conducting element connected between a third node of said signal transmission line and a second power supply node, and rendered conductive when a voltage at the third node exceeds a voltage level applied in a normal operation, the third node being located on said signal transmission line between the first node and said internal circuit.

6. The semiconductor device according to claim 5, wherein said second surge conducting element includes a PN junction coupled in a reverse direction viewed from the third node toward the second power supply node.

7. The semiconductor device according to claim 5, wherein said second surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to the second power supply node, and a second conduction node connected to the third node.

8. The semiconductor device according to claim 5, wherein said second surge conducting element includes a diode element connected to the third node in a reverse direction viewed from the third node.

9. The semiconductor device according to claim 1, further comprising a capacitor connected between the second node and said internal circuit.

10. The semiconductor device according to claim 1, further comprising a clamp circuit connected between the first power supply node and a second power supply node, for holding a voltage difference between the first and second power supply nodes so as not to exceed a prescribed voltage level.

11. The semiconductor device according to claim 10, wherein said clamp circuit clamps the voltage difference between the first and second power supply nodes to a voltage level lower than a breakdown voltage of a diffusion layer of a second conductivity type located on a surface of a substrate region of a first conductivity type.

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12. The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to the first power supply node, and a second conduction node connected to the second power supply node.

13. The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a back gate and a first conduction node connected together to the second power supply node, and a second conduction node connected to the first power supply node.

14. The semiconductor device according to claim 10, wherein said clamp circuit includes at least one first diode element connected between the first power supply node and the second power supply node in a forward direction viewed from the first power supply node, and at least one second diode element connected between the second power supply node and the first power supply node in a forward direction viewed from the second power supply node.

15. The semiconductor device according to claim 1, wherein the first power supply node is a ground node.

16. The semiconductor device according to claim 1, wherein said bypass transmission line is a quarter wavelength transmission line having a length substantially equal to one quarter of a wavelength at an operation frequency of said internal circuit.